Performance Analysis of Double Hetero-gate Tunnel Field Effect Transistor

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***Abstract*— A hetero gate dielectric low band gap material DG Tunnel FET is presented here. The investigated device is almost free from short channel effects like DIBL and V_t roll-off. Simulation of the device characteristics shows significant improvement over conventional double gate TFET when compared interms of on current, ambipolar current, roll-off, miller capacitance and, device delay time. Simulation is done using TCAD tools.**

***Index Terms*— band-to-band tunneling, hetero material, ambipolar current, miller capacitance**

I. Introduction

Semiconductor devices are scaled to achieve higher packing density, higher on current etc. However, the subthreshold swing is not scaled. As a result, it becomes difficult to turn the device off. As such, it becomes more vulnerable to noise [1]. At the same time, in order to maintain a high on current with reduced off state leakage, a reduction of subthreshold swing is required and has become one of the most important technological issues. MOSFETS are based on drift and diffusion mode of carrier transport where subthreshold swing depends on thermal voltage and at the least it can be . Therefore, a device can be designed which uses other mode of carrier transport so that a lower subthreshold can be achieved. The other modes are based on impact ionization and interband tunneling [2]-[3]. In our device we have considered interband tunneling. However, devices based on this mechanism fail to meet the ITRS requirements [4] it has been proposed to use double gate technology in conjunction with hetero gate dielectric. The double gate tunnel FET is based on band-to-band tunneling [5]-[7]. We have investigated a double gate hetero dielectric TFET with low band gap material. This device has several superior properties compared to conventional double gate silicon TFET.

The total gate capacitance of Tunnel FET consists of gate-to-source capacitance, gate-to-drain capacitance and quantum capacitance of the channel [8]. The gate to source capacitance $\left(C_{gs}\right)$ for conventional double gate silicon TFET is very low in the ON state and gate to drain capacitance or Miller capacitance $\left(C_{gd}\right)$ is very large due to little potential drop between the channel and drain [9]. In the OFF state, C_{gd} dominates since source to channel barrier resistance is large compare to that of drain to channel [9]. The quantum capacitance originates from filling the channel density of states from source and drain reservoirs [8]-[9]. To meet ITRS requirement and reduced Miller capacitance hetero gate oxide with low band gap material germanium is used.

II. Device structure And operation

The structure of the proposed device is as shown in Fig. 1. The basic structure is a p-i-n double gate device operating under reverse bias condition. It can operate both in n and p channel modes [3]. In p mode, $V_{gs} < V_F$ and in n mode, $V_{gs} > V_F$, where V_F is a reference voltage required to align the P^+ valence band and channel conduction band. In n-channel mode, tunneling occurs in the source side while in p-channel mode, tunneling occurs in the drain side. An electron inversion layer is created in the channel at the interface with the gate dielectric when a gate voltage greater is applied. Tunneling takes place from the source valence band to the conduction band in the inversion layer of the channel [10]. As mentioned, we have used heterogate dielectric. A low-K gate oxide (SiO_2 with dielectric constant 3.9) at the drain side and high-K oxide (HfO_2 with dielectric constant 25) at the tunneling junction are used. To reduce the ambipolar current at the drain side, low-K gate oxide is used.

Figs. 2 and 3 show the band diagram of the n-channel TFET in the ON and OFF states. In the OFF state, the potential barrier between the source and channel is so wide that no tunneling occurs even though a very small leakage current exists. In the on state, when the gate voltage exceeds the threshold voltage the potential barrier between the source and channel becomes narrower and a significant tunneling current flows [11].

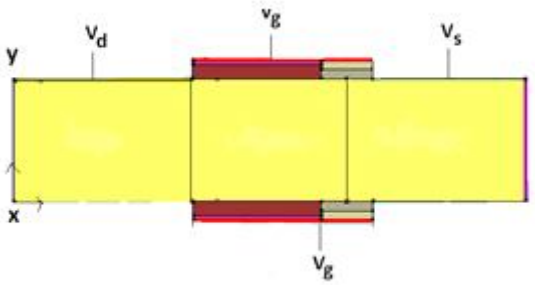

Fig. 1. Hetero Double gate-dielectric TFET

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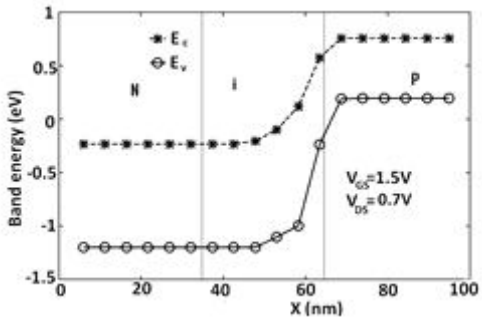

Fig. 2. Tunneling takes place when gate voltage is applied. The graph is plotted at y=2 nm

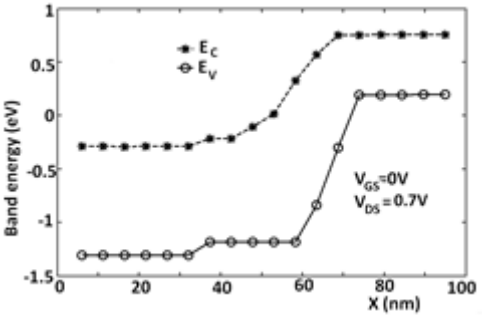

Fig. 3. At V_{GS} = 0 V , tunneling doesn't take place, at y=2 nm

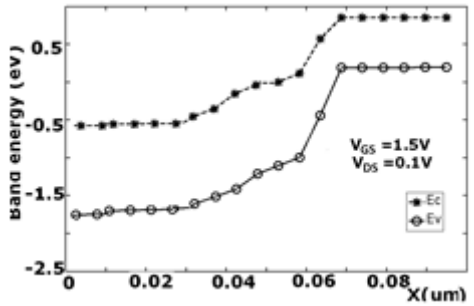

Fig. 4. Tunneling width remains same at V_{DS} = 0.7 and 0.1 V for the proposed device at y= 2nm

In a conventional TFET, as the thickness of the oxide layer is decreased, the tunneling current from gate starts flowing. This not only adversely affects the device performance but also increases the standby power of a VLSI chip. To decrease the effective oxide thickness (EOT) at the tunnel junction, high-K gate oxide is used so that the gate leakage, i.e. the gate tunneling current is reduced [12]. Metal gate with work function 4.5eV is used. A low band gap material (germanium) is used to increase the tunneling probability as tunneling probability is a function of band gap E_g [13]. The tunneling probability is calculated by Wentzel-Kramers-Brillouin (WKB) method [13]. Furthermore, low band gap material has reduced density of states. To operate this device, source is grounded, 1.5 V is applied to the gates, and drain is connected to 0.7 V.

As the gate voltage increases above V_F , the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow. In this device tunneling takes place at the source channel junction. This device has 25 nm channel length, body layer thickness t_s = 25 nm , oxide thickness 3 nm for SiO_2 and 2 nm for HfO_2 for double gate TFET. Length of SiO_2 is 25 nm and that of HfO_2 is 10 nm. High-K gate oxide near the tunneling junction increases the coupling between gate and tunneling junction. A high doping level, yet still realistic in terms of a design to be fabricated. In this paper, the doping concentration of source, drain, and channel are 10^{21} , 5×10^{18} , and 10^{17} cm^{-3} , respectively. The abrupt doping profile is used here.

III. RESULT AND DISCUSSIONS

Simulation is done using Synopsys TCAD Tools based on non local mesh band-to-band tunneling model [14]. Doping dependent mobility model is used. Bandgap narrowing is also activated. The length of high-K is optimized to minimize ambipolar current as shown in Fig. 5. When the length of high-K is 10 nm, the minimum ambipolar current is obtained. Ambipolar current is defined at $V_{GS} = -0.1V$ and $V_{DS} = 0.7V$. Using high-K material as a gate insulator may increase leakage current (I_{amb}) due to severe ambipolar behaviour. This behavior is due to the impact of phonon scattering thereby reducing mobility. The simulated device features different gate insulators at the source (high-K material) and drain (low-K) sides. Since gate-to-channel coupling strength is different between channel regions overlapped by the high-*k* material like HfO_2 and silicon oxide, Hetero Gate TFETs have a local minimum of *Ec* at the tunneling junction, which improves *I*on and SS. An abrupt on-off state transition is seen instead of the gradual transition exhibited by the tunnel FET between on-off states. The abrupt transition is more for 10 nm high-K. Characteristics of the proposed device have been compared with the conventional DG TFET. Simulation results, shown in Figs. 6 and 7, show improved I_D vs. V_{GS} characteristics of our device. The proposed device has better on current, off sate characteristics in comparison to conventional Si TFET. The actual value of SS in MOSFET is much higher than 60 mV/dec which results in increased I_{off} and thus become a major concern for low standby power (LSTP) digital applications [15]-[16]. Our device is a heterogate dielectric to achieve steeper subthreshold slope. Tunneling takes place from valence band of the P^+ source to the intrinsic channel conduction band. The tunneling occurs due to the application of gate voltage which reduces tunneling gap and creates very high local electric field. The current is governed by tunneling even though the electrons from intrinsic region move toward drain by drift-diffusion mechanism.

In this paper, the effects of scaling of the proposed TFET on subthreshold swing and threshold voltage roll-off have also been investigated. These characteristics of the conventional double gate TFET and proposed device are compared.

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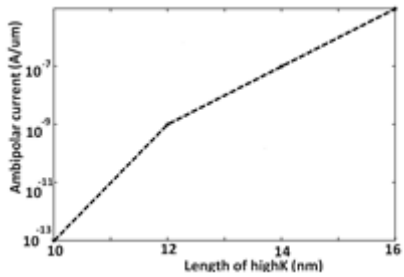

Fig.5 Ambipolar current is measured at 30 nm gate length

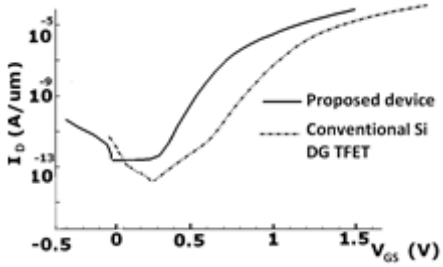

Fig. 6 log I_D vs. V_{GS} curve is plotted for proposed device and conventional device (30 nm gate length) at V_{DS}=0.7V

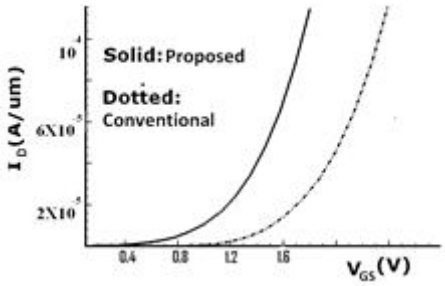

Fig. 7 I_D - V_{GS} curve for conventional device and proposed device, V_{DS} =0.7V

The gate length of the conventional as well as our device is varied and the corresponding SS values are plotted in Fig. 8. The proposed device has steeper and low subthreshold slope when it is closer to the off state $(V_{GS} \approx 0\ \mathrm{V})$, while its subthreshold slope is relatively large and less steeper when it operates near the on state $(V_{GS} = 1.5\ \mathrm{V})$. The plots shown in Fig. 8 use the average of these two values of the subthreshold slope. As seen, the average SS for the proposed device is 53 mV/dec for 30 nm gate length. It is also seen that gate length scaling provides better subthreshold swing. The high local electric field near the tunneling junction is responsible for sharp band bending and hence low subthreshold swing.

As seen from the energy band diagrams (Figs. 2 – 4), the tunnel bandgap almost remains unaltered to applied drain voltages. Thus, from the energy band point of view also we can conclude that the device is almost free from DIBL effect.

Furthermore, the use of low band gap material reduces the channel to drain capacitance [8]. The reduced channel to drain capacitance limits the Miller capacitance. However, the dominant component of C_{gg} is the C_{gd}. This is due to the basic tunnel FET structure. But the capacitance for the proposed structure is significantly lower compared to the conventional Si TFET. The quantum capacitance can also be scaled with reduced density of states. The hetero gate dielectric low band gap material DG tunnel FET has higher on current and reduced tunneling mass. The gate capacitance in the proposed device is limited by its reduced density of states compared to conventional silicon DG TFET, as show in Figs 10 and 11. The intrinsic device delay (τ) depends on $C_{gg}V_{DD} / I_{on}$ [9], where V_{DD} is the supply voltage.

Threshold voltage (V_t) roll-off for the proposed and conventional devices is compared in Fig. 9. The magnitude of gate threshold voltage is defined here using constant current method, with threshold set at $I_d = 10^{-7}$ A/m, when $V_{DS} = 0.7V$. Practically, the threshold voltage of our device is invariant to the applied drain voltage. It is shown in Fig. 9 that at and the value of threshold voltages at different gate lengths upto 45 nm are same. At higher gate lengths little mismatch is observed . This is due to the fact that the on off transition is less at at 50 nm gate length. Again the increased coupling between the gate and the channel contributes for such a highly desired result, as it is favorable for low standby power applications [3].

TABLE I. COMPARISON OF DELAY TIME

Type of TFET	I_{on}	C_{gg} (normalized)	(τ)
Conventional Si DG TFET	0.01mA	0.61	62pS
Hetero Ge DG TFET	1.01mA	0.42	4pS

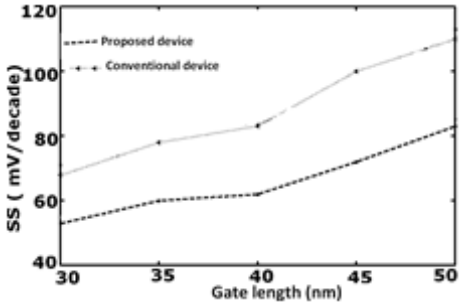

Fig. 8 SS versus gate lengths (nm) are plotted

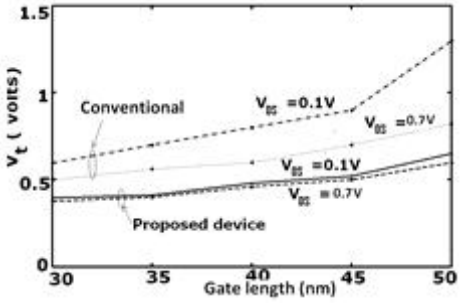

Fig.9 V_t roll-off for proposed device is negligible

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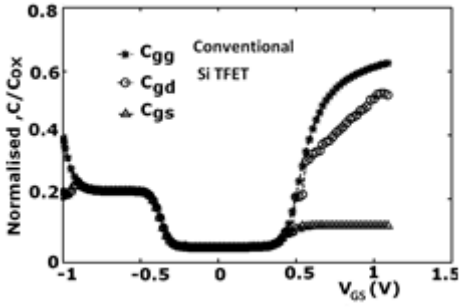

Fig.10 Variation of capacitances with V_{GS} for conventional DG TFET at V_{DS}=0.7V

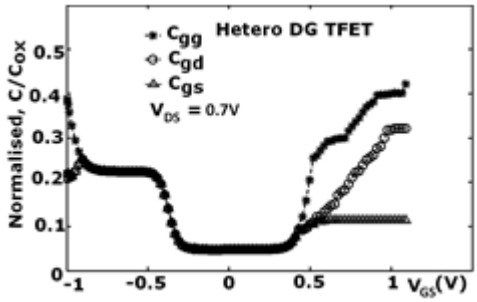

Fig.11 Variation of capacitances with V_{GS} for hetero gate low band gap DG TFET

Conclusions

A hetero gate dielectric double gate tunnel FET with low band gap materia.l shows significant improvement over conventional Si Double gate TFET. This proposed device has 53mV/dec subthreshold swing, on current in the range of mA, better immunity to short channel effects, reduced miller capacitance and low dynamic power consumption. This device is suitable for low power analog as well as digital applications.

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